

●General Description

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. It combines one N-channel MOSFET and one P-channel MOSFET.

●Features

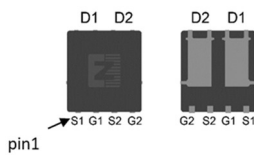
- Low $R_{DS(ON)}$ to minimize conductive loss
- Dual die in one package
- Low thermal resistance
- AEC-Q101 qualified

●Application

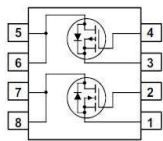
- BLDC motor driver
- Load switch



●Product Summary



DFN5*6



$V_{DS1}=40V$

$V_{DS2}=-40V$

$R_{DS(ON)1}=8mR$

$R_{DS(ON)2}=12mR$

$I_{D1}=38A$

$I_{D1}=-33A$



●Ordering Information

Part NO.	ZMCA88401N
Marking	ZMC88401
Packing information	REEL TAPE
Basic ordering unit (pcs)	3000

●N-Channel Absolute Maximum Ratings ($T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Drain-source voltage	V_{DS}		-	40	V
Gate-source voltage ^①	V_{GS}		-20	20	V
Continuous drain current	I_D	$V_{GS}=10V, T_C=25^{\circ}C$	-	38	A
	I_D	$V_{GS}=10V, T_C=75^{\circ}C$	-	32	A
	I_D	$V_{GS}=10V, T_C=100^{\circ}C$	-	27	A
Pulsed drain current ^①	I_{DM}	Pulsed; $t_p \leq 10 \mu s; T_C = 25^{\circ}C$;	-	114	A
Total power dissipation	P_D	$T_C=25^{\circ}C$	-	39	W
Total power dissipation	P_D	$T_A=25^{\circ}C$	-	3.3	W
Operating junction temperature	T_J		-55	175	$^{\circ}C$
Storage temperature	T_{STG}		-55	175	$^{\circ}C$
Single pulse avalanche energy	E_{AS}	$L=0.1mH, V_{GS}=10V, R_g=25\Omega$,	-	40	mJ
		$L=0.5mH, V_{GS}=10V, R_g=25\Omega$,	-	84	mJ

ESD level (HBM)		CLASS 1C
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● P-Channel Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Drain-source voltage	V_{DS}		-	-40	V
Gate-source voltage ^①	V_{GS}		-20	20	V
Continuous drain current	I_D	$V_{GS}=-10\text{V}$, $T_C=25^{\circ}\text{C}$	-	-33	A
	I_D	$V_{GS}=-10\text{V}$, $T_C=75^{\circ}\text{C}$	-	-27	A
	I_D	$V_{GS}=-10\text{V}$, $T_C=100^{\circ}\text{C}$	-	-24	A
Pulsed drain current ^①	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_C = 25^{\circ}\text{C}$;	-	-99	A
Total power dissipation	P_D	$T_C=25^{\circ}\text{C}$	-	39	W
Total power dissipation	P_D	$T_A=25^{\circ}\text{C}$	-	3.3	W
Operating junction temperature	T_J		-55	175	$^{\circ}\text{C}$
Storage temperature	T_{STG}		-55	175	$^{\circ}\text{C}$
Single pulse avalanche energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=-10\text{V}$, $R_g=25\Omega$,	-	60	mJ
		$L=0.5\text{mH}$, $V_{GS}=-10\text{V}$, $R_g=25\Omega$,	-	108	mJ
ESD level (HBM)				CLASS 2	

● Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	3.8	$^{\circ}\text{C/W}$
Thermal resistance, junction - ambient ^②	R_{thJA}	-	-	45	$^{\circ}\text{C/W}$
Soldering temperature(total time<10s)	T_{sold}	-	-	260	$^{\circ}\text{C}$

● N-Channel Electronic Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	1.3	1.7	2.5	V
Drain-source leakage current	I_{DSS}	$V_{GS}=0\text{V}$, $V_{DS}=40\text{V}$	-	-	1	μA
Gate- source leakage current	I_{GSS}	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	-	-	± 100	nA
Static drain-source on resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=8\text{A}$, $T_J=25^{\circ}\text{C}$	-	8	12	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=6\text{A}$, $T_J=25^{\circ}\text{C}$	-	13	17	m Ω
Forward transconductance	g_{FS}	$V_{DS}=5\text{V}$, $I_{SD}=8\text{A}$	-	11	-	S

Diode forward voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=8A$	-	-	1.3	V
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● N-Channel Dynamic Characteristics ($T_j=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f = 1MHz, V_{DS}=25V, V_{GS}=0V$	-	1930	-	pF
Output capacitance	C_{oss}		-	154	-	pF
Reverse transfer capacitance	C_{rss}		-	110	-	pF
Gate resistance	R_g	$f = 1MHz$	-	1.4	-	Ω
Total gate charge	Q_g	$V_{DD} = 15V, I_D = 20A, V_{GS} = 10V$	-	30	-	nC
Total gate charge	$Q_{g(4.5V)}$		-	16	-	nC
Gate-source charge	Q_{gs}		-	5.4	-	nC
Gate-drain charge	Q_{gd}		-	5.9	-	nC
Turn-on delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G = 3.3\Omega, I_D = 20A$	-	8	-	ns
Turn-on rise time	t_r		-	2.5	-	ns
Turn-off delay time	$t_{D(off)}$		-	41	-	ns
Turn-off fall time	t_f		-	8	-	ns
Reverse recovery time	t_{rr}	$V_{DD}=20V, dI_S/dt = 100A/us, I_S=20A$	-	11	-	ns
Reverse recovery charge	Q_{rr}		-	13	-	nC

● P-Channel Electronic Characteristics ($T_j=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250uA$	-40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250uA$	-1.3	-1.7	-2.5	V
Drain-source leakage current	I_{DSS}	$V_{GS}=0V, V_{DS}=-40V$	-	-	-1	μA
Gate- source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Static drain-source on resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-8A, T_j=25^{\circ}C$	-	12	17	m Ω
		$V_{GS}=-4.5V, I_D=-6A, T_j=25^{\circ}C$	-	20	24	m Ω
Forward transconductance	g_{FS}	$V_{DS}=-5V, I_{SD}=-8A$	-	18	-	S
Diode forward voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=-8A$	-	-	-1.3	V

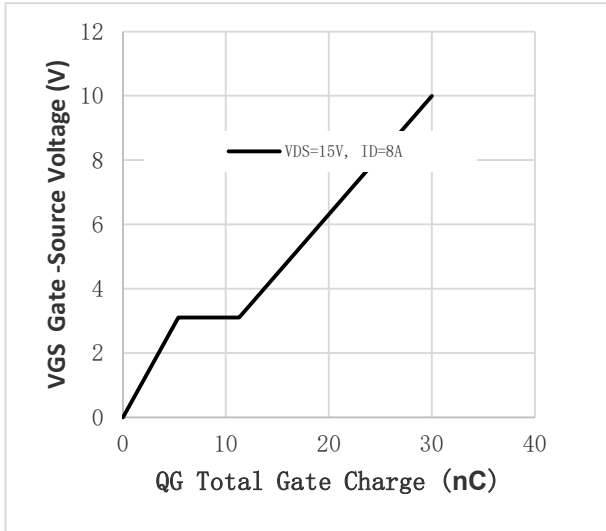
● P-Channel Dynamic Characteristics ($T_j=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f = 1MHz, V_{DS}=-25V, V_{GS}=0V$	-	3430	-	pF
Output capacitance	C_{oss}		-	262	-	pF
Reverse transfer capacitance	C_{rss}		-	206	-	pF

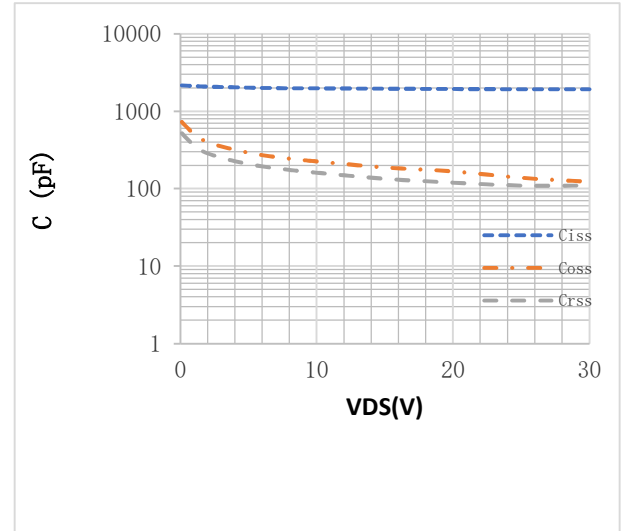
Gate resistance	R_g	$f = 1\text{MHz}$	-	8.6	-	Ω
Total gate charge	Q_g	$V_{DD} = -15\text{V}, I_D = -10\text{A},$ $V_{GS} = -10\text{V}$	-	56	-	nC
Total gate charge	$Q_{g(-4.5V)}$		-	25	-	nC
Gate-source charge	Q_{gs}		-	7.6	-	nC
Gate-drain charge	Q_{gd}		-	10.8	-	nC
Turn-on delay time	$t_{D(on)}$	$V_{GS} = -15\text{V}, V_{DS} = -10\text{V},$ $R_G = 3.3\Omega, I_D = -20\text{A}$	-	20	-	ns
Turn-on rise time	t_r		-	174	-	ns
Turn-off delay time	$t_{D(off)}$		-	43	-	ns
Turn-off fall time	t_f		-	10.4	-	ns
Reverse recovery time	t_{rr}	$V_{DD} = -20\text{V}, dI_S/dt = -$ $100\text{A}/\mu\text{s}, I_S = -20\text{A}$	-	58	-	ns
Reverse recovery charge	Q_{rr}		-	75	-	nC

●N-Channel Characteristics Curve ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

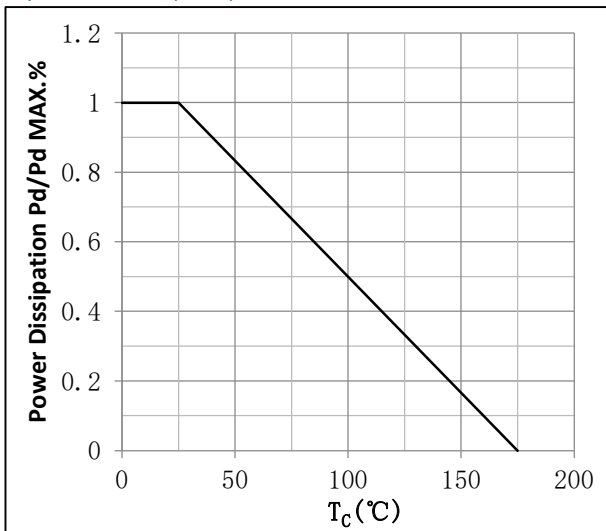
●Fig.1 Gate-source voltage as a function of gate charge;
Typical values; $T_J=25^{\circ}\text{C}$



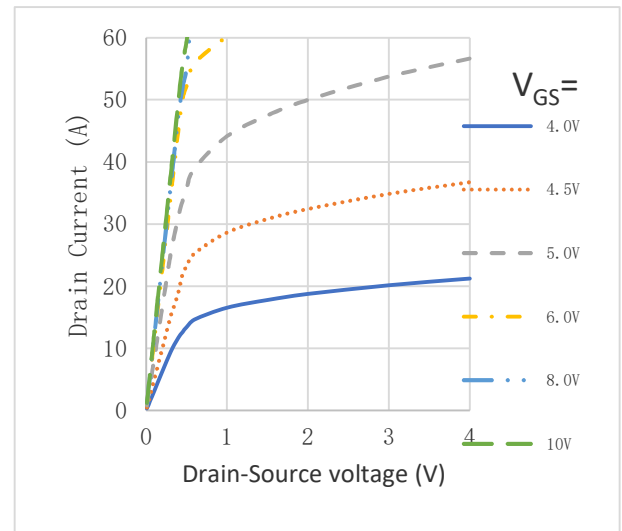
●Fig.2 Input, output and reverse transfer capacitances as a function of drain-source voltage; Typical values; $T_J=25^{\circ}\text{C}$



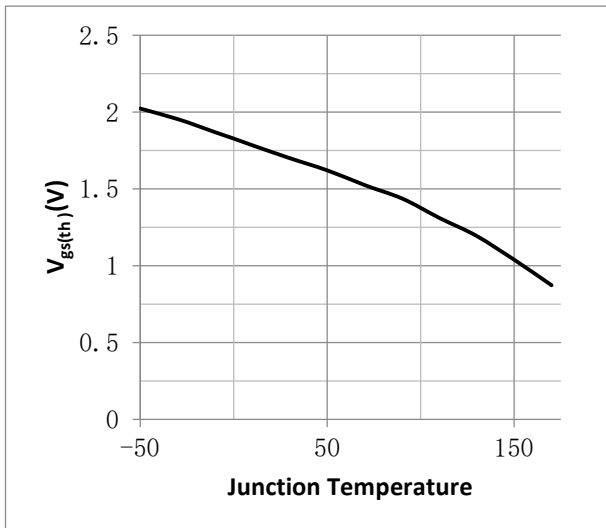
●Fig.4 Normalized total power dissipation as a function of case temperature; Calculative values Normalized Power Dissipation = $P_d/P_d(25^{\circ}\text{C})$



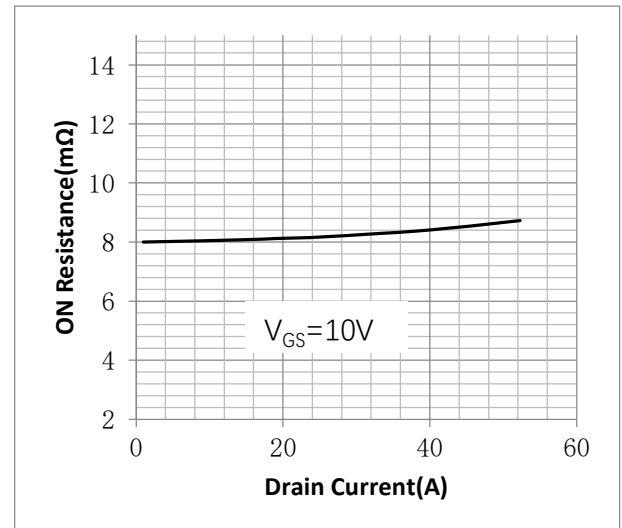
●Fig.4 Output characteristics: drain current as a function of drain-source voltage; Typical values; $T_J=25^{\circ}\text{C}$



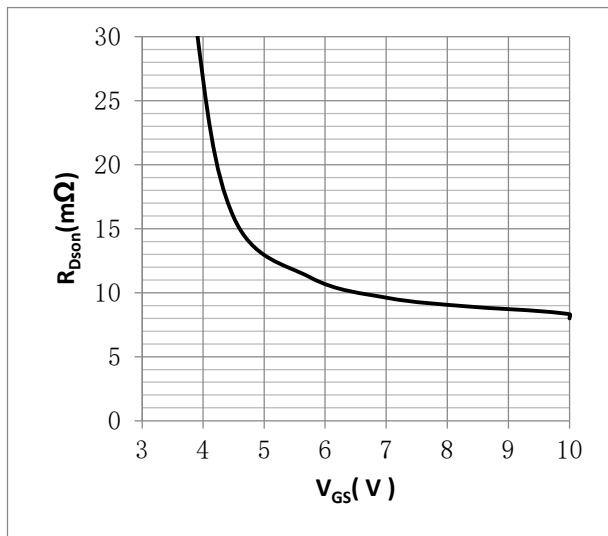
●Fig.5 Gate-source threshold voltage as a function of junction temperature; Typical values



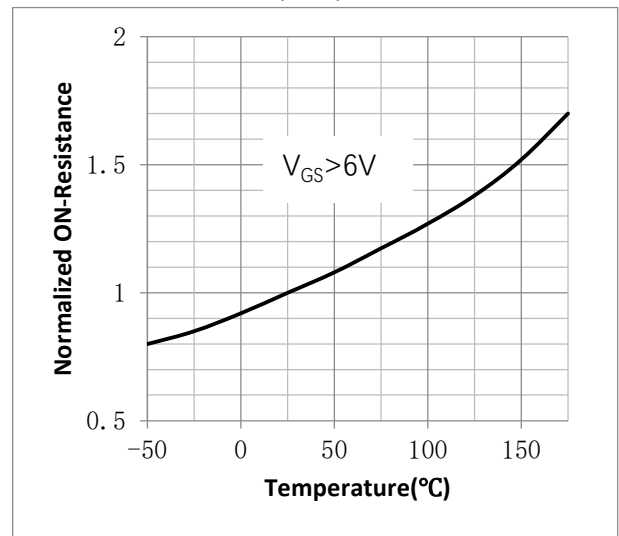
●Fig.6 Drain-source on-state resistance as a function of drain current; Typical values; $T_J=25^{\circ}\text{C}$



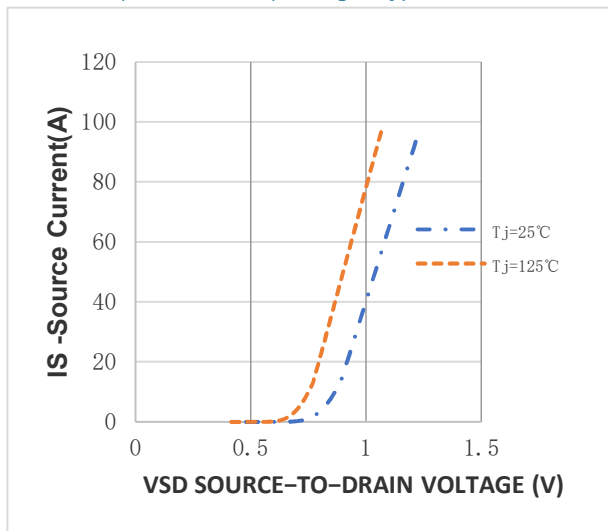
● Fig.7 Drain-source on-state resistance as a function of gate-source voltage; Typical values



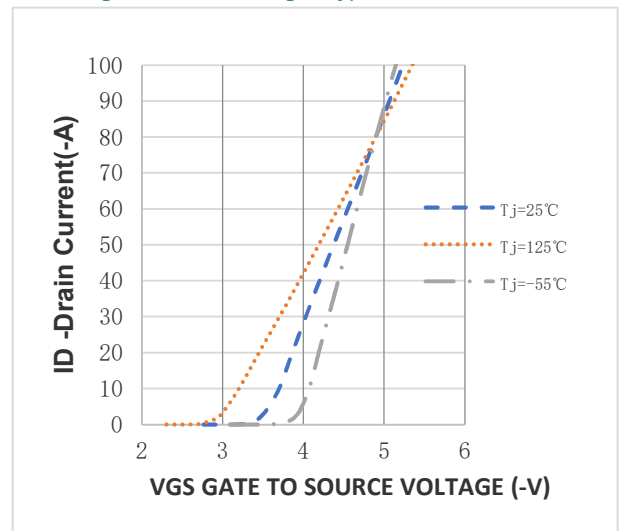
● Fig.8 Normalized drain-source on-state resistance factor as a function of junction temperature; Typical values Normalized On-Resistance= $R_{DS(on)}/R_{DS(on)}(25^{\circ}\text{C})$



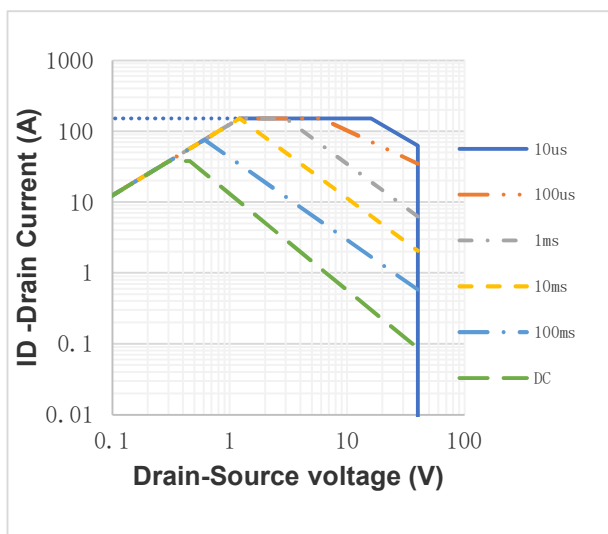
● Figure 9. Source (diode forward) current as a function of source-drain (diode forward) voltage; Typical values



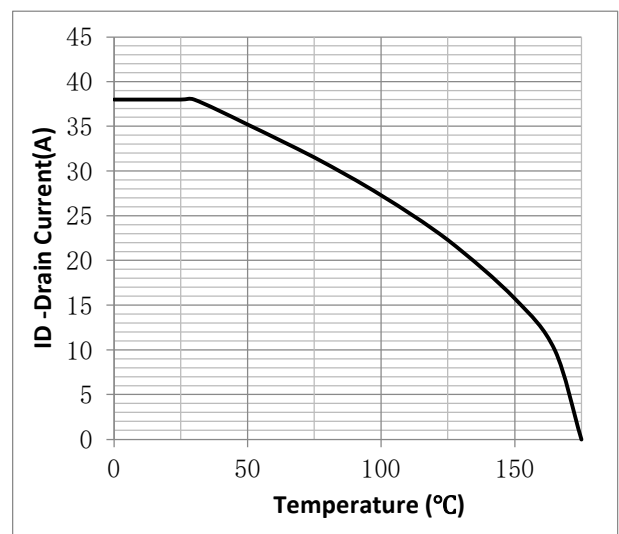
● Figure 10. Transfer characteristics: drain current as a function of gate-source voltage; Typical values



● Fig.11 Safe operating area: continuous and peak drain currents as a function of drain-source voltage; Calculative values

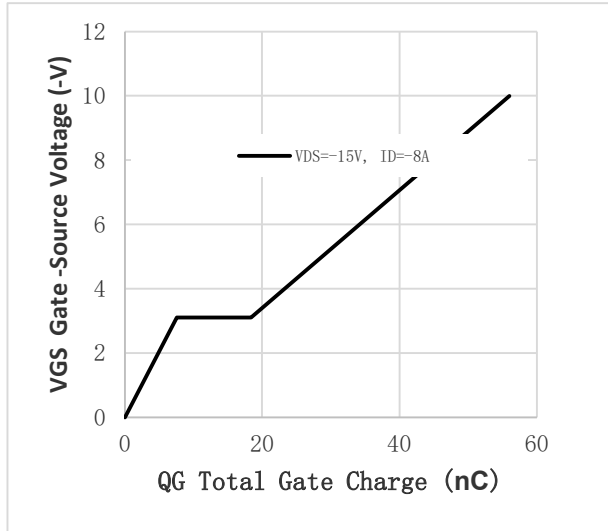


● Fig.12 Continuous drain current as a function of case temperature³; Calculative values

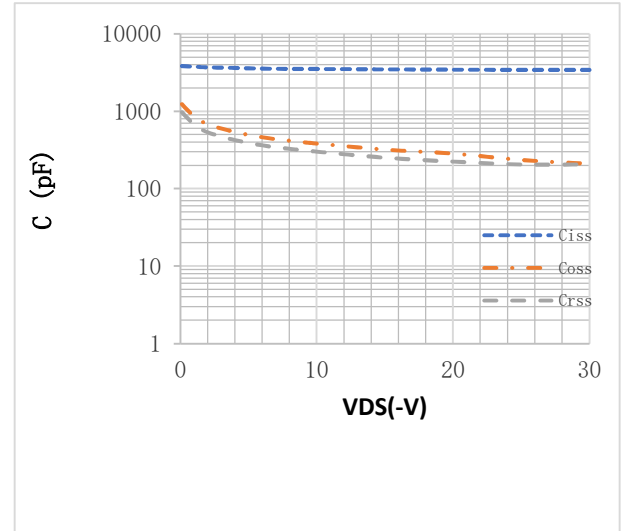


●P-Channel Characteristics Curve ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

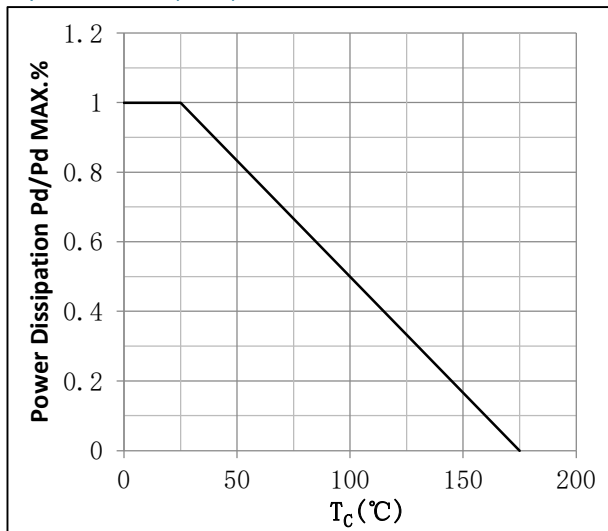
●Fig.1 Gate-source voltage as a function of gate charge; Typical values; $T_J=25^{\circ}\text{C}$



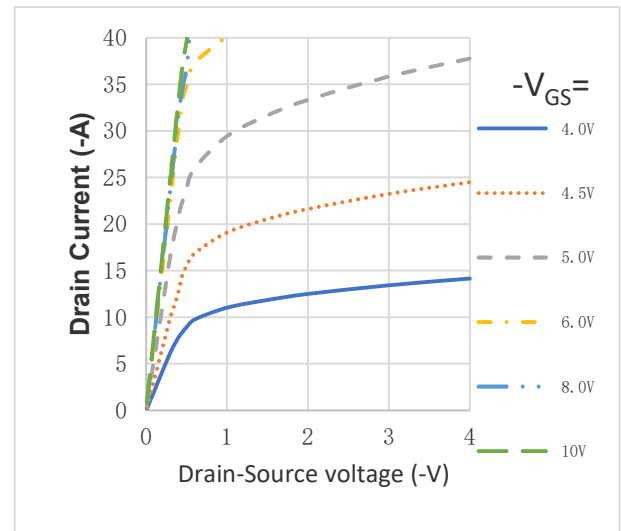
●Fig.2 Input, output and reverse transfer capacitances as a function of drain-source voltage; Typical values; $T_J=25^{\circ}\text{C}$



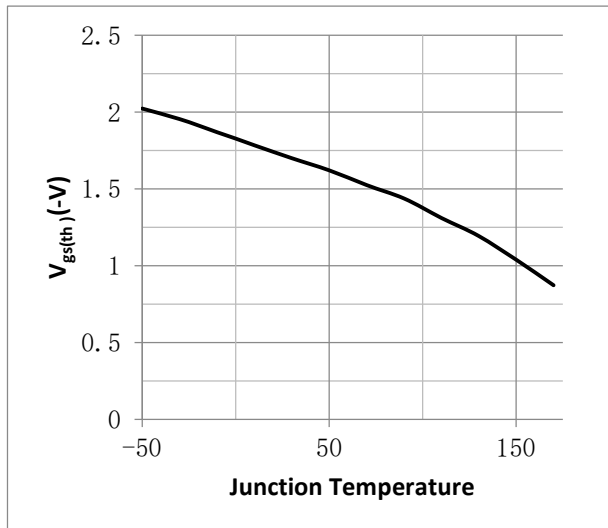
●Fig.3 Normalized total power dissipation as a function of case temperature; Calculative values Normalized Power Dissipation = $P_d/P_d(25^{\circ}\text{C})$



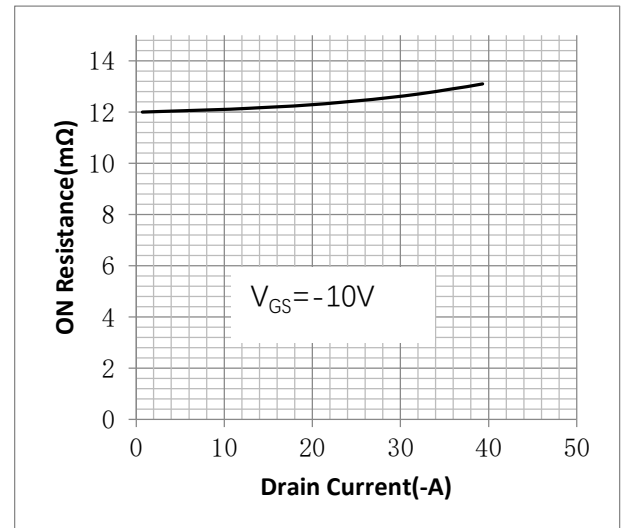
●Fig.4 Output characteristics: drain current as a function of drain-source voltage; Typical values; $T_J=25^{\circ}\text{C}$



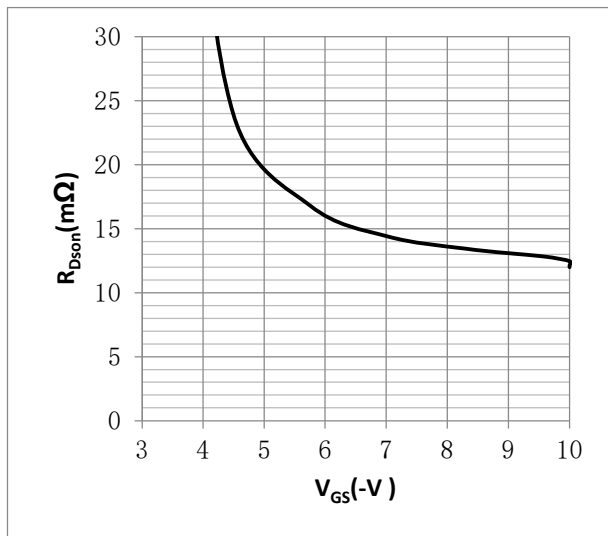
●Fig.5 Gate-source threshold voltage as a function of junction temperature; Typical values



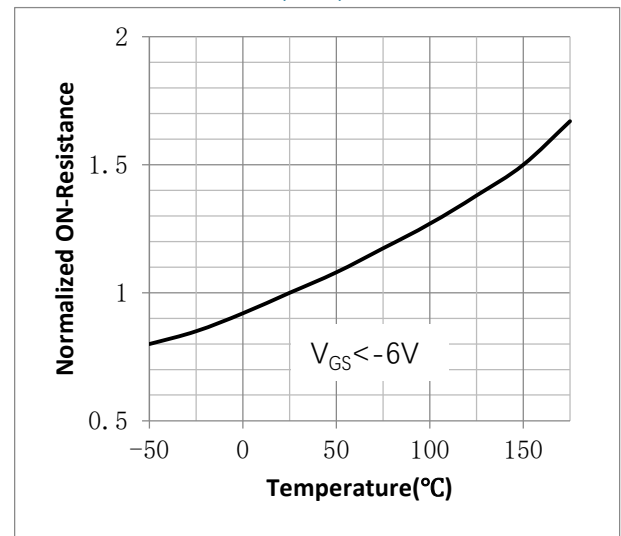
●Fig.6 Drain-source on-state resistance as a function of drain current; Typical values; $T_J=25^{\circ}\text{C}$



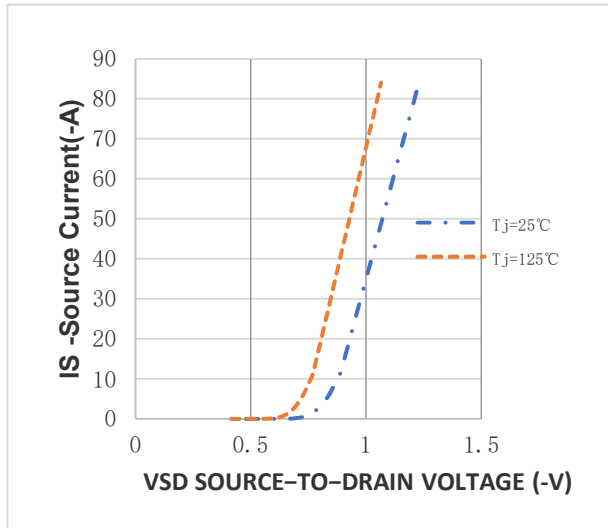
● Fig.7 Drain-source on-state resistance as a function of gate-source voltage; Typical values



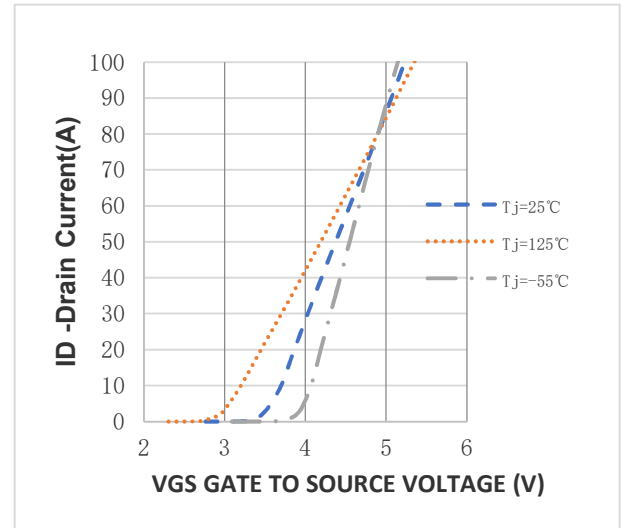
● Fig.8 Normalized drain-source on-state resistance factor as a function of junction temperature; Typical values Normalized On-Resistance= $R_{DS(on)}/R_{DS(on)}(25^{\circ}\text{C})$



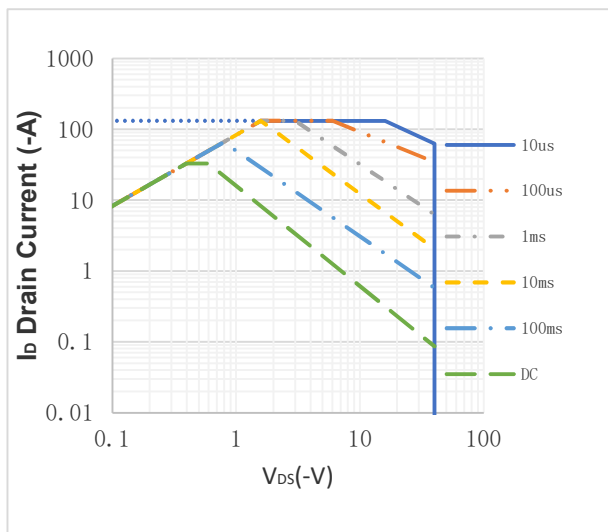
● Figure 9. Source (diode forward) current as a function of source-drain (diode forward) voltage; Typical values



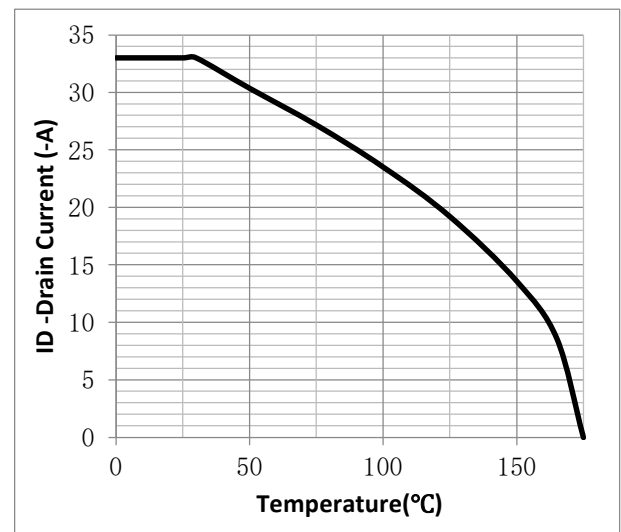
● Figure 10. Transfer characteristics: drain current as a function of gate-source voltage; Typical values



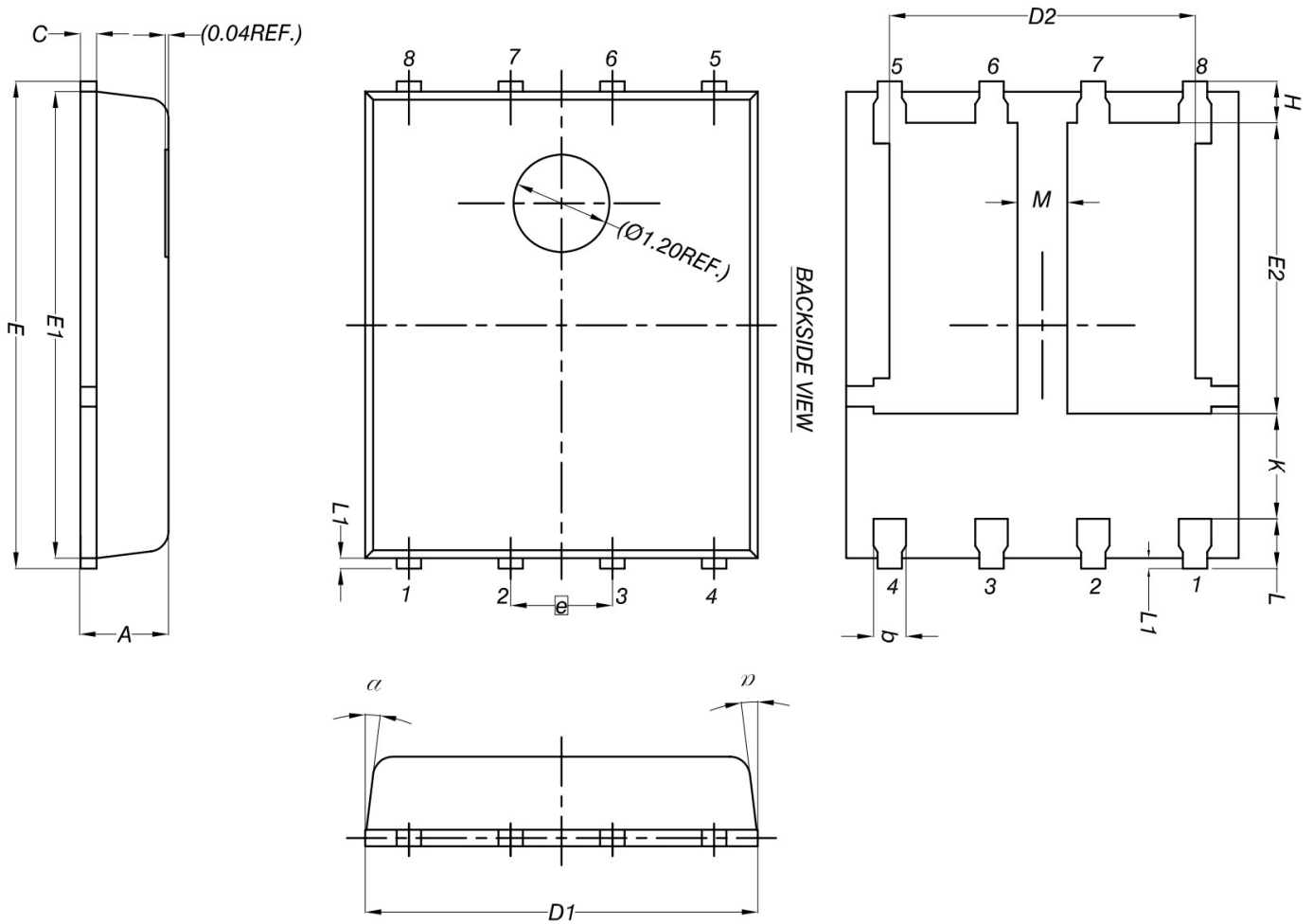
● Fig.11 Safe operating area: continuous and peak drain currents as a function of drain-source voltage; Calculative values



● Fig.12 Continuous drain current as a function of case temperature³; Calculative values

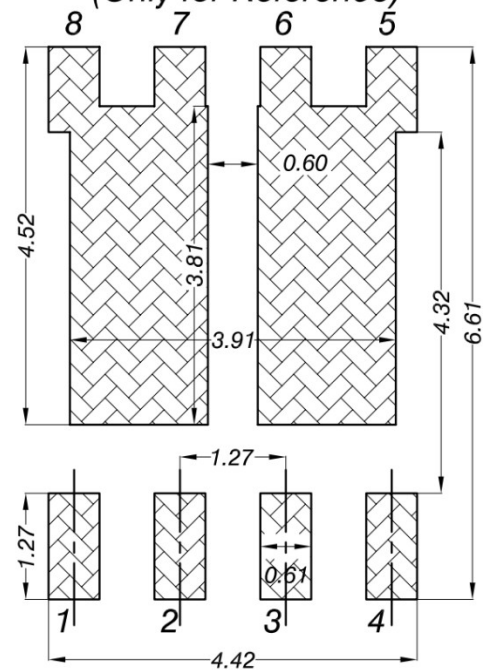


Package Outline



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
α	0°	-	12°

Land Pattern
(Only for Reference)



● Note

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_J=175^{\circ}C$, $t=1000$ hours; For DC, the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_J=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$ (N-channel)/
-10V(P-channel).

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● Revision History

Version	Date	Change
A	2021.10.16	New
B	2021.11.12	Modified the ID curve
C	2022.12.5	Add Dynamic Characteristics, correct the marking.
D	2023.11.21	Add Vgs>6v in the curve, correct ID
E	2025.9.17	P channel fig.12 corrected